IN THE CLAIMS:

Please cancel Claim 52 without prejudice or disclaimer of subject matter.

Please amend Claim 22 as shown below.

1 to 21. (Cancelled)

22. (Currently Amended) A method for manufacturing a semiconductor device in which a plurality of electro-thermal conversion elements and a plurality of insulated gate type field effect transistors for flowing electric currents through said plurality of electro-thermal conversion elements are integrated on a first conductive type semiconductor substrate, said method comprising the steps of:

forming a second conductive type first semiconductor region on one principal surface of the first conductive type semiconductor substrate;

forming a gate insulator film on said first semiconductor region;

forming a first gate electrode on said gate insulator film;

doping a first conductive type impurity by utilizing said first gate electrode as a mask;

forming a second semiconductor region for providing a channel region of an insulated gate type field effect transistor of said plurality of insulated gate type field effect transistors, by diffusing said first conductive type impurity; and

~~forming (a)~~ forming a second conductive type source region on the surface side of said second semiconductor region ~~by utilizing said first gate electrode as a mask~~

~~such that said source region extends from beneath said first gate electrode to beneath a second gate electrode formed on said gate insulator film and (b) a~~ and a second conductive type drain region on the surface side of said first semiconductor region,

wherein said source region is formed by utilizing said first gate electrode as a mask such that said source region extends from beneath said first gate electrode to beneath a second gate electrode formed on said gate insulator film,

wherein said source region is formed by ion implantation of an impurity from a direction inclined at a predetermined angle from a direction normal to the first conductive type semiconductor substrate, and

wherein said drain region is formed with a mask to offset said drain region from said first gate electrode.

23. (Cancelled)

24. (Previously Presented) A method according to claim 22, further comprising the steps of:

performing a first conductive type ion implantation through an area between said first and second gate electrodes into at least a channel region put between said source region and said first semiconductor region on the surface side of said second semiconductor region after said step of forming said second semiconductor region; and

performing a heat treatment for electrically activating an impurity implanted by said first conductive type ion implantation.

25. (Previously Presented) A method according to claim 22, further comprising the steps of:

performing a first conductive type ion implantation through an area between said first and second gate electrodes into at least a channel region put between said source region and said first semiconductor region on the surface side of said second semiconductor region after said step of forming said second semiconductor region; and

performing a heat treatment for electrically activating an impurity implanted by said first conductive type ion implantation,

wherein said first conductive type ion implantation is ion implantation in which ions of boron are implanted in energy of 100 keV or more.

26. (Previously Presented) A method according to claim 22, wherein said drain region is provided in plurality, at least two of said plurality of drain regions being connected with the same one of said plurality of electro-thermal conversion elements, and wherein said source region is provided in plurality, each of said plurality of source regions being connected with one another.

27 to 52. (Cancelled)